THAT WHICH IS CLAIMED IS:

1. A method of correcting soft errors in a content addressable memory (CAM) device, comprising the steps of:

performing a plurality of consecutive search operations on a plurality of CAM array blocks within the CAM device during foreground operations while concurrently internally correcting soft errors in groups of entries read from idle ones of the plurality of CAM array blocks during background operations.

2. The method of Claim 1, wherein each of the entries in a group includes a check word of length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$ and N is a logical width of the entries.

3. The method of Claim 1, wherein the plurality of CAM array blocks are static CAM (SCAM) array blocks.

4. The method of Claim 1, wherein each of the groups of entries is a horizontal group of entries that are read in parallel from a plurality of idle CAM array blocks.

5. A method of correcting soft errors in a static content addressable memory (SCAM) device having a plurality of SCAM array blocks therein, said method comprising the steps of:

reading at least a first entry from an idle one of the plurality of SCAM array blocks;

internally correcting an error in the first entry while simultaneously searching one or more of the plurality of SCAM array blocks; and

writing an error-corrected version of the first entry into the plurality of SCAM array blocks.

6. The method of Claim 5, wherein said reading step comprises

reading a horizontal or vertical group of entries from idle ones of the plurality of SCAM array blocks during a group read operation.

7. The method of Claim 6, wherein said reading step comprises simultaneously searching active ones of the plurality of SCAM array blocks.

8. The method of Claim 6, wherein said step of internally correcting an error comprises correcting a soft error in the first entry using a check word of length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$ and N is a logical width of the first entry.

9. A method of operating a static content addressable memory (SCAM) device having a plurality of SCAM array blocks therein, said method comprising the steps of:

searching active ones of the plurality of SCAM array blocks while simultaneously internally correcting a soft error in an entry previously read from a first one of the plurality of SCAM array blocks during a background mode of operation.

10. The method of Claim 9, wherein said searching step comprises searching active ones of the plurality of SCAM array blocks while simultaneously correcting soft errors in a group of entries previously read from one or more of the plurality of SCAM array blocks during a vertical or horizontal group read operation.

11. The method of Claim 10, wherein the step of correcting soft errors comprises correcting a soft error in the entry using a check word of length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$ and N is a logical width of the entry.

12. The method of Claim 5, wherein the step of correcting a soft error comprises correcting a soft error in a global mask word previously read from a row of global mask cells.

13. The method of Claim 6, wherein the step of correcting a soft error is followed by the step of writing the entry with a corrected soft error into the first one of the plurality of SCAM array blocks, while simultaneously searching another one of the plurality of SCAM array blocks.

14. The method of Claim 6, wherein the step of correcting a soft error is followed by the step of writing the entry with a corrected soft error into the first one of the plurality of SCAM array blocks, while simultaneously writing to or reading from another one of the plurality of SCAM array blocks.

15. A content addressable memory (CAM) device, comprising:

at least one CAM array block comprising a first row having CAM cells, at least one check bit cell and at least one flag cell therein, said at least one flag cell configured to designate a valid or invalid status of a respective check bit(s) retained by the at least one check bit cell.

16. The CAM device of Claim 15, wherein said at least one CAM array block has a logical width of N CAM cells; and wherein the check word retained by the at least one check bit cell in the first row has a length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$.

17. The CAM device of Claim 15, wherein said at least one CAM array block further comprises a second row of dedicated global mask cells and check bit cells.

18. The CAM device of Claim 17, wherein the global mask cells in the second row are configured to retain first and second global masks that each have a logical width of N bits; and wherein a check word retained by the check bit cells in the second row has a length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$.

19. The CAM device of Claim 17, wherein the check bit cells in the second row are configured to be less susceptible to soft errors relative to the CAM cells in the first row by virtue of the fact that latching inverters within the check bit cells are larger than latching inverters within the CAM cells.

20. A content addressable memory (CAM) device, comprising:

at least one CAM array block having a row of CAM cells and check bit cells therein, said row having a logical width that supports a search word width of N-bits, where $2^c \geq 2N+c+1 \geq 2^{c-1}$ and "c" is a length of a check word retained by the check bit cells.

21. The CAM device of Claim 20, wherein each of a plurality of CAM cells in said row comprises first and second memory cells; and wherein each of a plurality of the check bit cells in said row comprises a respective check bit memory cell that is configured to be less susceptible to soft errors relative to the first and second memory cells by virtue of the fact that latching inverters within the check bit memory cell are larger than latching inverters in the first and second memory cells.

22. The CAM device of Claim 20, wherein a pair of check bit cells within the row comprise a 4T compare circuit.

23. The CAM device of Claim 20, wherein said at least one CAM array block comprises a row having dedicated global mask cells and check bit cells therein.

24. The CAM device of Claim 23, wherein the dedicated global mask cells are configured to retain first and second global masks that each have a logical width of N bits.

25. The CAM device of Claim 24, wherein the dedicated global mask cells each comprise four transistors that are configured to support reading of respective bits of the first and second global masks.

26. A static content addressable memory (SCAM) device, comprising:

at least one SCAM array block having a row of binary SCAM cells and check bit cells therein, said row having a logical width of N-bits, where $2^c \geq N+c+1 \geq 2^{c-1}$ and "c" is a length of a check word retained by the check bit cells.

27. The SCAM device of Claim 26, wherein said at least one SCAM array block comprises at least one row having dedicated global mask cells and check bit cells therein.

28. The CAM device of Claim 27, wherein the dedicated global mask cells are configured to retain first and second global masks that each have a logical width of N bits.

29. The CAM device of Claim 28, wherein the dedicated global mask cells each comprise four transistors that are configured to support reading of respective bits of the first and second global masks.

30. A static content addressable memory (SCAM) device, comprising:

at least one SCAM array block having at least one row of SCAM cells therein, said at least one row comprising a plurality of memory cells that are configured to store a check word of sufficient length to enable the correction of at least one soft error said at least one row.

31. The SCAM device of Claim 30, wherein the length "c" of the check word is sufficient to meet the following relationship: $2^c \geq N_d+N_m+c+1 \geq 2^{c-1}$, where N_d equals the number of active data cells in said at least one row and N_m equals the number of active mask cells in said at least one row.

32. The SCAM device of Claim 31, wherein each of a plurality of the SCAM cells in said at least one row comprises a pair of memory cells that share a common word line.

33. The SCAM device of Claim 30, wherein each of a plurality of the SCAM cells in said at least one row comprises a pair of memory cells that share a common word line.

34. The SCAM device of Claim 30, wherein the length "c" of the check word is sufficient to meet the following relationship: $2^c \geq 2N+c+1 \geq 2^{c-1}$, where N is a logical width of said at least one SCAM array block.

35. The SCAM device of Claim 31, wherein c = 8, N_d is about 80 and N_m is about 80.

36. A method of operating a content addressable memory (CAM) device having a plurality of CAM array blocks therein, said method comprising the steps of:

reading a group of entries from one or more of the plurality of CAM array blocks, during a horizontal or vertical group read operation;

correcting at least one soft error in the group of entries during a background operation while at least one of the plurality of CAM array blocks is undergoing a foreground operation; and

writing an entry that has been corrected for soft errors during the background operation into one of the plurality of CAM array blocks.

37. The method of Claim 36, wherein each of the entries in the group

comprises data, mask and check bits; and wherein said reading step comprises reading data, mask and check bits in parallel from one of the plurality of CAM array blocks.

38. The method of Claim 37, wherein each of the entries in the group comprises a check word having a length "c" that is sufficient to meet the following relationship: $2^c \geq N_d+N_m+c+1 \geq 2^{c-1}$, where N_d equals the number of data bits in the entry and N_m equals the number of mask bits in the entry.

39. The method of Claim 36, wherein each of the entries in the group comprises a check word having a length "c" that is sufficient to meet the following relationship: $2^c \geq 2N+c+1 \geq 2^{c-1}$, where N is a logical width of the plurality of CAM array blocks.

40. The method of Claim 36, wherein the foreground operation is selected from the group consisting of search, write and read operations.

41. A content addressable memory (CAM) device, comprising:

at least one CAM array block having a plurality of consecutive rows of dedicated global mask cells therein, with each of the plurality of rows of dedicated global mask cells comprising a respective plurality of memory cells that are configured to store a check word of sufficient length to enable the correction of at least one soft error in at least one global mask stored in the corresponding row of dedicated global mask cells.

42. A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks; and

a dedicated check bit memory array that is configured to retain check bit words associated with entries in said plurality of CAM array blocks.

43. The CAM device of Claim 42, wherein said plurality of CAM array blocks have rows therein that comprise check bit cells, which are

configured to retain parity information.

44. An integrated circuit memory cell array, comprising:

a row having data bit memory cells and check bit memory cells therein that are configured to be less susceptible to soft errors relative to the data bit memory cells by virtue of the fact that latching inverters within the check bit memory cells are larger than latching inverters within the data bit memory cells.

45. A content addressable memory (CAM) device, comprising:

at least one CAM array block having a plurality of rows of ternary and/or quaternary CAM cells therein, with each of the plurality of rows comprising a plurality of check bit memory cells that are configured to support a check word having a length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$ and N equals a logical width of the at least one CAM array block.

46. A method of operating a static content addressable memory (SCAM) device, comprising the steps of:

searching a SCAM array block in the SCAM device while simultaneously internally correcting a soft error in a data entry previously written into the SCAM device; and

rewriting the corrected data entry into the SCAM array block.

47. A method of operating a content addressable memory (CAM) device having a plurality of CAM array blocks therein, said method comprising the steps of:

searching active ones of the plurality of CAM array blocks while simultaneously internally correcting a soft error in an entry previously read from a first one of the plurality of CAM array blocks during a vertical or horizontal group read operation.

48. The method of Claim 47, wherein the step of correcting a soft error comprises correcting a soft error in the entry using a check word of length "c", where $2^c \geq 2N+c+1 \geq 2^{c-1}$ and N is a logical width of the entry.

49. The method of Claim 48, wherein the plurality of CAM array blocks comprise ternary and/or quaternary CAM cells.

50. The method of Claim 49, wherein the entry comprises N data bits and N local mask bits.

51. The method of Claim 50, wherein the step of correcting a soft error comprises correcting a soft error in the N local mask bits.

52. The method of Claim 47, wherein the step of correcting a soft error is followed by the step of writing the entry with the corrected soft error into the first one of the plurality of CAM array blocks, while simultaneously searching another one of the plurality of CAM array blocks.

53. The method of Claim 47, wherein the step of correcting a soft error is followed by the step of writing the entry with the corrected soft error into the first one of the plurality of CAM array blocks, while simultaneously writing to or reading from another one of the plurality of CAM array blocks.

54. A content addressable memory (CAM) device, comprising:

at least one CAM array block comprising a first row of memory cells therein, said first row of memory cells comprising:

a plurality of CAM cells;

at least one check bit cell; and

at least one flag cell that is configured to designate a valid or invalid status of a check bit retained by said at least one check bit cell.

55. A content addressable memory (CAM) device, comprising:

a CAM array block having at least one row therein that comprises a plurality of CAM cells and a dual-function check bit cell pair that is configurable as a CAM cell when necessary to account for a defective CAM cell in the at least one row.

56. The CAM device of Claim 55, wherein the at least one row comprises a plurality of dedicated check bit cells that are not configurable as CAM cells.

57. The CAM device of Claim 56, wherein at least some of the dedicated check bit cells are configured to retain parity data.

58. The CAM device of Claim 56, wherein a first dedicated check bit cell is configured to be less susceptible to soft errors relative to a check bit cell in the dual-function check bit cell pair by virtue of the fact that latching inverters within the first dedicated check bit cell are larger than latching inverters within the check bit cell in the dual-function check bit cell pair.

59. The CAM device of Claim 56, wherein the at least one row comprises at least one redundant check bit cell.

60. The CAM device of Claim 55, wherein each of the plurality of CAM

cells comprises at least one SRAM memory cell having a first pair of inverters therein that define a first latch; wherein the at least one row comprises a dedicated SRAM check bit cell having a second pair of inverters therein that define a second latch; and wherein the second pair of inverters are larger than the first pair of inverters.

61. An array of content addressable memory (CAM) cells, comprising:

a row of CAM cells having at least one check bit cell therein that is electrically coupled to a match line associated with said row.

62. The array of Claim 61, further comprising a pseudo-ground line electrically connected to the at least one check bit cell.

63. The array of Claim 61, wherein the at least one check bit cell comprises XOR logic that is electrically coupled to a pair of differential data lines.

64. The array of Claim 61, wherein said row of CAM cells comprises a plurality of dedicated check bit cells that are not electrically coupled to the match line.

65. The array of Claim 64, wherein at least one of the plurality of dedicated check bit cells comprises a redundant check bit cell.

66. The array of Claim 61, wherein the at least one check bit cell is configured to be less susceptible to soft errors relative to the CAM cells by virtue of the fact that latching inverters within the at least one check bit cell are larger than latching inverters in the CAM cells.

67. The array of Claim 61, further comprising a row of dedicated global mask cells.

68. The array of Claim 67, wherein said row of dedicated global mask cells comprises at least one check bit cell.

69. A method of operating a content addressable memory (CAM) array having a column of check bit cells therein that are electrically coupled to a plurality of match lines, said method comprising the steps of:

searching the CAM array while simultaneously globally masking the column of check bit cells.

70. A content addressable memory (CAM) device, comprising:

a group of rows of ternary CAM cells that each comprise $c(m^{-1})$ active check bit cells therein, where m is the number of rows within said group, c is a length of a check word that applies to said group, N is a logical width of each row within said group and $2^c \geq m(2N)+c+1 \geq 2^{c-1}$.

71. A method of correcting soft errors in a content addressable memory (CAM) device, comprising the steps of:

reading an entry from an idle one of a plurality of CAM array blocks in the CAM device while simultaneously searching another one of the plurality of CAM array blocks; and then

checking the entry to detect the presence or absence of a soft error therein.

72. The method of Claim 71, wherein the entry comprises a plurality of check bits; and wherein said checking step is followed by the step of correcting the soft error within the entry using error correction circuitry within the CAM device.

73. The method of Claim 72, wherein said checking and correcting steps are performed while the one of the plurality of CAM array blocks is idle.

74. The method of Claim 73, wherein said correcting step is followed by the step of writing the entry into the one of the plurality of CAM array blocks.

75. The method of Claim 71, wherein said reading step comprises reading a horizontal group of entries from idle ones of the plurality of CAM array blocks; and wherein said checking step comprises checking the group of entries for soft errors using error checking circuitry within the CAM device.

76. The method of Claim 71, wherein said reading step comprises reading a horizontal group of entries in parallel from idle ones of the plurality of CAM array blocks; and wherein said checking step comprises checking the group of entries for soft errors using error checking circuitry within the CAM device.

77. The method of Claim 71, wherein the plurality of CAM array blocks are static CAM array blocks.

78. A method of correcting soft errors in a static random access memory (SRAM) device, comprising the steps of:

systematically reading and internally correcting soft errors in entries within the SRAM device during a background mode of operation while concurrently reading entries from and/or writing new entries to the SRAM device during a foreground mode of operation.

79. A content addressable memory (CAM) device, comprising:

a plurality of CAM array blocks;

a control circuit that is configured to respond to a write operation by:

writing a new word into a row(s) of a CAM array block;

reading a plurality of words that are associated with the row(s) from one or more of the plurality of CAM array blocks;

generating a check bit word that supports correction of at least one error in a combined word that comprises the new word and the plurality of words; and

storing the check bit word in the CAM device.

80. The CAM device of Claim 79, wherein said control circuit is configured to store the check bit word by writing the check bit word or portion thereof into one of the plurality of CAM array blocks.

81. The CAM device of Claim 79, wherein said control circuit is configured to store the check bit word by writing the check bit word into a check bit memory within the CAM device.

82. An integrated circuit memory device, comprising:

a plurality of memory array blocks;

a control circuit that is configured to respond to a write operation by:

writing a new word into a row(s) of a memory array block;

reading a plurality of words that are associated with the row(s) from one or more of the plurality of memory array blocks;

generating a check bit word that supports correction of at least one error in a combined word that comprises the new word and the plurality of words; and

storing the check bit word in the memory device.

83. The memory device of Claim 82, wherein said control circuit is configured to store the check bit word by writing the check bit word or portion thereof into one of the plurality of memory array blocks.

84. The CAM device of Claim 82, wherein said control circuit is configured to store the check bit word by writing the check bit word into a check bit memory within the memory device.